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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/984,562	12/03/1997	JEFFREY S. MAILLOUX	95-0653.02	2303

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EXAMINER
KIM, HONG CHONG

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/984,562	MAILLOUX ET AL.	
	Examiner	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-32,59,61 and 63-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *65* is/are allowed.

6)☒ Claim(s) *22-32,59,61,63 and 66-72* is/are rejected.

7)☒ Claim(s) *64* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *26* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1. Claims 22-32, 59, 61, 63-65, and 66-72 are presented for examination. Claim 60 has been canceled. This office action is in response to the Amendment filed on 7/2/02.

2. Receipt is acknowledged of information disclosure statement filed on 9/3/02, which the statement has been placed of record in the file. Information disclosed and listed on PTO 1449 was considered.

3. It is noted that this application appears to claim subject matter disclosed in the co-pending section of this application. Applicants are reminded to maintain a clear line of demarcation between this application and co-pending applications to avoid possible double patenting.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 22-32, 59, 61, and 66-72 are rejected under 35 USC 102(e) as being anticipated by *Manning*, U.S. Patent 5,610,864.

As to claims 22 and 66, *Manning* discloses the invention as claimed. *Manning* discloses

a memory circuit, comprises control logic (Fig. 1 Refs. 36 & 38 and col.6 lines 26-32); selection (Fig. 1 Refs. 36 & 38 and col.6 lines 26-32) and temporary storage circuit (Fig. 1 Ref. 26, col. 4 lines 23-25 and col. 5 lines 8-10); and a multiplexer for receiving the first external address and the selected mode control (Fig. 1 Ref. 26, controlling the column address counter/latch between burst and pipeline reads on this limitation, because during the burst operation, the addresses is incremented internal to the device, col. 3 lines 19-21, however, during the pipelined operation, each column address is provided one access per cycle, col. 5 line 43-50, in other words, during the burst internal counter/latch path is selected however, during the pipelined mode external counter/latch path is selected, see also col. 6 lines 26-34) and for switching the memory circuit between a burst mode (col. 6 lines 14-34 and col. 7 lines 43-54) and a pipelined mode (col. 5 lines 43-50, "the current invention include a pipelined architecture" and "switching between standard fast page mode (non-EDO) and burst mode" read on this limitation, in other words, in order to work in the pipeline architecture one has to select pipeline mode).

As to claims 23-24 and 67-68, Manning. further discloses external mode select signal and enable signal (Fig. 1 Ref 38 and col.6 lines 14-32).

As to claims 25 and 69, Manning. further discloses write enable and output enable (Fig. 2, WE & OE).

As to claim 26, Manning. further discloses a counter (Fig. 1 Ref. 26).

As to claim 27, Manning. further discloses the counter is used in the burst mode (col. 4 lines 47-49 and col. 8 line 67).

As to claim 28, *Manning* further discloses a second external address (col. 5 lines 43-50, Fig.2 row & col addresses).

As to claim 29, Manning. further discloses EDO modes (col. 4 line 50), pipeline mode (col. 5 lines 43-50), and burst mode (col. 7 lines 28+).

As to claims 30 and 31, Manning further discloses no CAS delay latency during a write cycle (col. 5 lines 66+) and at least a two CAS latency during read cycle (col. 7 lines 36-37).

As to claim 32, Manning further discloses an asynchronously accessible memory array (Fig. 1 and EDO constitutes asynchronous memory, col. 6 lines 14-16).

As to claim 70, Manning further discloses an output enable signal (Fig. 1 Ref. 42).

As to claim 71, Manning. further discloses a counter (Fig. 1 Ref. 26) and incrementing

the first external address when in the burst mode (col. 3 lines 17-24).

As to claim 72, Manning. further discloses EDO modes (col. 4 line 50), pipeline mode (col. 5 lines 43-50), and burst mode (col. 7 lines 28+).

As to claim 59, *Manning* discloses a memory circuit (Fig. 1), comprises control logic (Fig. 1 Refs. 36 & 38 and col.6 lines 26-32); selection (Fig. 1 Refs. 36 & 38 and col.6 lines 26-32) and temporary storage circuit (Fig. 1 Ref. 26) and a first external address (Fig. 1 Ref. 26, col. 4 lines 23-25 and col. 5 lines 8-10); a multiplexer for receiving the first external address ans the selected mode control (Fig. 1 Ref. 26, controlling the column address counter/latch between burst and pipeline reads on this limitation, because during the burst operation, the addresses is incremented internal to the device, col. 3 lines 19-21, however, during the pipelined operation, each column address is provided one access per cycle, col. 5 line 43-50, in other words, during the burst mode, internal counter/latch path is selected however, during the pipelined mode external counter/latch path is selected, see also col. 6 lines 26-34) and for switching the memory circuit between a burst mode (col. 6 lines 14-34 and col. 7 lines 43-54) and a pipelined mode (col. 5 lines 43-50, "the current invention include a pipelined architecture" and "switching between standard fast page mode (non-EDO) and burst mode" read on this limitation, in other words, in order to work in the pipeline architecture one has to select pipeline mode), wherein the memory circuit is an asynchronous dynamic random access memory circuit (Fig. 1 and EDO

constitutes asynchronous memory, col. 6 lines 14-16).

As to claim 61, *Manning* disclose the invention as claimed in claim 22. *Manning* further discloses control logic for providing an internal mode control signal (Fig. 1 Ref. 40, col. 3 lines 17-25, col. 4 lines 46-50, col. 5 lines 9-12 and col. 6 lines 30-40).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 22-32, 59, 61, 63, and 66-72 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Manning*, U.S. Patent 5,729,503 (503) *in view of Manning*, U.S. Patent 5,610,864 (864).

As to claim 63, *Manning (503)* disclose the invention as claimed. *Manning (503)* discloses a memory circuit, comprises control logic for providing a selected mode control signal (Fig. 1 Refs. 36 & 38 and col.5 lines 13-14); selection and temporary storage circuit (Fig. 5) and a first external address (Fig. 5 Ref. 305); a first multiplexer (Fig. 5 Ref. 350); a second external address (Fig. 5 Ref. 320); a second multiplexer (Fig. 5 Ref. 370); and the control logic for switching the memory circuit between a burst mode and a page mode (col. 10 lines 17-32). .

Although 503 discloses control logic for burst and normal page, 503 does not specifically disclose a pipeline mode. However it was well known in the memory art at the time the invention was made to use the pipeline mode to access memory per each cycle thereby increasing the access speed. For example, Manning (864) discloses a pipelined mode (col. 5 lines 43-50) for he purpose of increasing the throughput by accessing data per every cycle (col 5 lines 46-48) thereby increasing the system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify a page mode of 503 with a pipelined mode of 864 because it would increase the throughput by accessing data per every cycle thereby increasing the system throughput.

As to claims 22 and 66, *Manning (503) and Manning (864)* discloses the invention as claimed above.

Manning (503) further discloses selection and temporary storage circuit (Fig. 5 col 10 lines 1-32); and a multiplexer (Fig. 5 Ref. 350) for receiving the first external address (Fig. 5 Ref. 16) and the selected mode control (col. 10 lines 16-32) and for switching the memory circuit between a burst mode and a page mode (col. 10 lines 16-32).

Manning (864) further discloses a memory circuit, comprises control logic (Fig. 1 Refs. 36 & 38 and col.6 lines 26-32); and circuit for switching the memory circuit between a burst mode (col. 6 lines 14-34 and col. 7 lines 43-54) and a pipelined mode (col. 5 lines 43-50, "the

current invention include a pipelined architecture" and "switching between standard fast page mode (non-EDO) and burst mode" read on this limitation, in other words, in order to work in the pipeline architecture one has to select pipeline mode).

As to claims 23-24 and 67-68, Manning (503). further discloses external mode select signal and enable signal (Fig. 1 Ref 38 and col. 6 lines 14-33).

As to claims 25 and 69, Manning (503). further discloses write enable and output enable (Fig. 2, WE and OE).

As to claim 26, Manning (503). further discloses a counter (Fig. 1 Ref. 26).

As to claim 27, Manning (503). further discloses the counter is used in the burst mode (col. 10 lines 20-32).

As to claim 28, *Manning (503)* further discloses a second external address (Fig. 5 Ref. 320, Fig.2 row & col addresses).

As to claim 29, Manning (864). further discloses EDO modes (col. 4 line 50), pipeline mode (col. 5 lines 43-50), and burst mode (col. 7 lines 28+).

As to claims 30 and 31, Manning (503) further discloses no CAS delay latency during a write cycle (col. 4 lines 66+) and at least a two CAS latency during read cycle (col. 6 lines 37-41).

As to claim 32, Manning (503) further discloses an asynchronously accessible memory array (Fig. 1 and EDO constitutes asynchronous memory, abstract).

As to claim 70, Manning (503) further discloses an output enable signal (Fig. 1 Ref. 42).

As to claim 71, Manning (503). further discloses a counter (Fig. 1 Ref. 26) and incrementing the first external address when in the burst mode (col. 4 lines 50-62).

As to claim 72, Manning (864). further discloses EDO modes (col. 4 line 50), pipeline mode (col. 5 lines 43-50), and burst mode (col. 7 lines 28+).

As to claim 59, *Manning (503) and Manning (864)* disclose the invention as claimed in claim 22. Manning (503). further discloses wherein the memory circuit is an asynchronous dynamic random access memory circuit (Fig. 1 and EDO constitutes asynchronous memory, abstract).

As to claim 61, *Manning (503) and Manning (864)* disclose the invention as claimed in claim 22. *Manning (503)* further discloses control logic for providing an internal mode control signal (col. 10).

Allowable Subject Matter

8. Claim 65 is allowed.

9. Claim 64 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

10. Applicant's arguments filed on 7/16/02 have been fully considered but they are not persuasive.

Applicant's argument on pages 6-8 that the reference does not disclose selecting between a burst mode and a pipeline modes of operations is not considered persuasive.

"The current invention include a pipelined architecture" (col. 5 lines 43-49 in Manning. '864) and "switching between standard fast page mode (non-EDO) and burst mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning, '864) read on this limitation, in other words, in order to work in the pipeline architecture one has to select pipeline mode. Also given the teachings of above reference one of the ordinary skill in the art at the time the invention was

made would have been lead to an obvious fashion to provide a pipelined page mode circuitry since Manning, '864 discloses that the current invention include a pipelined architecture (col. 5 lines 43-49) which would increase accessing speed.

Alternatively, *Manning (503)* discloses a memory circuit, comprises control logic for providing a selected mode control signal (Fig. 1 Refs. 36 & 38 and col.5 lines 13-14); selection and temporary storage circuit (Fig. 5) and a first external address (Fig. 5 Ref. 305); a first multiplexer (Fig. 5 Ref. 350); a second external address (Fig. 5 Ref. 320); a second multiplexer (Fig. 5 Ref. 370); and the control logic for switching the memory circuit between a burst mode and a page mode (col. 10 lines 17-32). Although 503 discloses control logic for burst and normal page, 503 does not specifically disclose a pipeline mode. However it was well known in the memory art at the time the invention was made to use the pipeline mode to access memory per each cycle thereby increasing the access speed. For example, Manning (864) discloses a pipelined mode (col. 5 lines 43-50) for he purpose of increasing the throughput by accessing data per every cycle (col 5 lines 46-48) thereby increasing the system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify a page mode of 503 with a pipelined mode of 864 because it would increase the throughput by accessing data per every cycle thereby increasing the system throughput.

Therefore, broadly written claims are disclose by the references cited.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

14. When responding to the office action, Applicants are advised to provide the examiner

with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

15. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

16. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
After-final (703) 746-7238
Official (703) 746-7239 (for formal communications intended for entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
October 21, 2002

HONG CHONG KIM
PRIMARY EXAMINER